WHAT IS CLAIMED IS:

1. A thin film semiconductor device comprising:

an insulating substrate; and

a plurality of thin film transistors of n-channel type and p-channel type formed on said insulating substrate each having a polycrystalline silicon film as an active layer;

wherein said thin film transistors of an identical channel type include plural classes of thin film transistors whose threshold voltages are different one another and wherein

said thin film transistors of different channel types include thin film transistors to which the same dopant are introduced into channel regions thereof at approximately with approximately an equal dose.

2. The thin film semiconductor device according to claim 1, wherein said plural classes of thin film transistors with different threshold voltages comprise a thin film transistor including p-type or n-type dopant in the channel region and a thin film transistor not including dopant in the channel region.

3. The thin film semiconductor device according to claim 1, wherein said plural classes of thin film transistors with different threshold voltages comprise a thin film transistor including p-type or n-type dopant in the channel region and a thin film transistor including both p-type and n-type dopants in the channel region.

4. The thin film semiconductor device according to claim 1, comprising at least an analog circuit unit requiring an idling current at

circuit operation time and a switch,

wherein said analog circuit unit includes a thin film transistor with a low threshold voltage, which is included in the plural classes of thin film transistors with different threshold voltages, on a current path of the idling current and wherein said switch is comprised of a thin film transistor with a high threshold voltage which is included in said plural classes of thin film transistors with different threshold voltages.

5. The thin film semiconductor device according to claim 4, wherein said analog circuit unit includes said switch on the current path of the idling current and said switch cuts off the idling current.

6. The thin film semiconductor device according to claim 5, wherein an activation and deactivation of said analog circuit unit is controlled by conduction and cutoff of the idling current via said switch.

7. The thin film semiconductor device according to claim 4, wherein, when said thin film transistor with the low threshold voltage is included in a current path route of the idling current among an input terminal, an output terminal, and power supply terminals, said analog circuit unit includes said switch in said current path route.

8. The thin film semiconductor device according to claim 4, wherein said thin film transistor with a high threshold voltage and said thin film transistor with a low threshold voltage are both of enhancement type.

9. The thin film semiconductor device according to claim 4, wherein said analog circuit part includes one of an amplifier circuit, a power supply circuit, and a comparator.

10. The thin film semiconductor device according to claim 4, wherein

said analog circuit unit is a differential amplifier circuit that at least includes said thin film transistor with the low threshold voltage in a differential pair and includes said switch in a current path route of said differential pair.

11. A display device comprising an insulating substrate; a display unit; and a circuit unit for driving said display unit; wherein said display unit and said circuit unit for driving said display unit are integrated on said insulating substrate; and

wherein said circuit unit includes the analog circuit unit and the switch as defined in claim 4.

12. A display device comprising:

an insulating substrate;

a circuit unit including an analog circuit unit, a logic circuit unit and a plurality of switches; and

a display unit;

wherein said circuit unit are configured by thin film transistors formed on a polycrystalline silicon film on said insulating substrate; and

wherein said analog circuit unit includes at least a thin film transistor whose threshold voltage is lower than the threshold voltage of thin film transistors used in said logic circuit unit.

13. The display device according to claim 12, wherein said analog circuit unit receives a power via said switch composed of a thin film transistor whose threshold voltage is equal to that of a thin film transistor used in said logic circuit unit.

14. The display device according to claim 12, wherein said display unit includes a plurality of pixel switches each composed of a thin film transistor whose threshold voltage is equal to that of a thin film transistor used in said logic circuit unit.

15. A method of manufacturing a thin film semiconductor device comprising the step of forming a plurality of n-channel thin film transistors and a plurality of p-channel thin film transistors using a polycrystalline silicon film on an insulating substrate,

said method further comprising the step of introducing p-type dopant or n-type dopant to a channel region of at least a part of said n-channel thin film transistors and at least a part of said p-channel thin film transistors at the same time.

16. A method of manufacturing a thin film semiconductor device comprising the step of forming a plurality of n-channel thin film transistors and a plurality of p-channel thin film transistors using a polycrystalline silicon film on an insulating substrate,

said method further comprising the steps of:

introducing p-type or n-type dopant to a whole region; and

introducing the n-type dopant or the p-type dopant to a channel region of at least a part of said n-channel thin film transistors and at least a part of said p-channel thin film transistors at the same time.

17. A thin film semiconductor device comprising:

an insulating substrate; and

a plurality of thin film transistors of an n-channel type and a p-channel type, each having a crystalline silicon film as an active layer

formed on the insulating substrate;

wherein said p-channel type thin film transistors and/or said n-channel type thin film transistors includes plural classes of thin film transistors whose threshold voltage are different one another; and

wherein there are provided, among said thin film transistors, at least pair of thin film transistors, each channel type being different and each having the same dopant introduced into a channel region with an equal dose.

18. A thin film semiconductor device comprising:

an insulating substrate; and

a plurality of thin film transistors being at least one type of an n-channel type and a p-channel type, each having a crystalline silicon film as an active layer formed on the insulating substrate;

wherein among said thin film transistors, there is at least one thin film transistor having a channel region into which dopant is introduced and at least one thin film transistor having a channel region into which dopant is not introduced.

19. A thin film semiconductor device according to claim 17, wherein at least one type thin film transistors of an n-channel type and a p-channel type are classified into more than 1 or more than 2 classes in regard to the magnitude of the threshold voltage.

20. A thin film semiconductor device comprising:

an insulating substrate; and

a plurality of thin film transistors of an n-channel type and a p-channel type, each having a crystalline silicon film as an active layer

on the insulating substrate; said plurality of thin film transistors of an n-channel type and/or a p-channel type being classified into a plurality of classes having different threshold voltage; wherein

among said thin film transistors there are at least one thin film transistor having a relatively low threshold voltage and at least one thin film transistor having a relatively high threshold voltage, inserted in series in a current path between terminals of power supplies and/or between terminal of the power supply and an input/output terminal; and wherein

said thin film transistor having a relatively high threshold voltage and being controlled to be turned on and off by a control signal supplied to a control terminal thereof, controls activation and deactivation of a circuit including said thin film transistor having a relatively low threshold value.

21. A differential amplifier circuit comprising:

a differential stage including:

a differential pair for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair connected between an output pair of the differential pair and a first power supply;

a current source connected between said differential pair and a second power supply and supplying a current to said differential pair;

said differential pair and/or said load element pair being comprised of transistors each having relatively low threshold value; and

a switch circuit inserted in a current path of said differential

stage for controlling an activation and deactivation of said differential stage, said switch circuit including at least one transistor which has a threshold value higher than that of the transistor having relatively low threshold value and which is controlled to be on and off by a control signal supplied to a control terminal thereof.

22. The differential amplifier circuit according to claim 21, wherein said switch circuit is comprised of a transistor connected in series with said current source between said differential pair and a second power supply, said transistor having a threshold value higher than that of the transistor having relatively low threshold value and including the control terminal for receiving the control signal to be controlled to be on and off, or,

said switch circuit is constituted by said current source comprised of a transistor having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a bias signal as said control signal to be controlled to be on and off.

23. The differential amplifier circuit according to claim 21, wherein there is provided a transistor constituting said switch circuit, having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a control signal to be controlled to be on and off for activating and inactivating said load element pair.

24. A differential amplifier circuit comprising:

a differential stage including:

a differential pair for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair connected between an output pair of the differential pair and a first power supply; and

a current source connected between said differential pair and a second power supply and supplying a current to said differential pair; and

an output amplification stage receiving an output of said differential stage and having an output terminal for outputting an output signal, said output amplification stage including an output stage transistor connected between said output terminal and said first power supply;

said differential pair and/or said load element pair being comprised of transistors each having relatively low threshold value;

a first switch circuit for controlling an activation and deactivation of said differential stage, wherein said switch circuit comprises a transistor connected in series with said current source between said differential pair and a second power supply, having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a control signal to be controlled to be on and off, or said first switch circuit is constituted by said current source comprised of a transistor having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a control signal to be controlled to be on and off;

a second switch circuit for controlling an activation and deactivation of said output amplification stage, including a transistor connected between the control terminal of said output stage transistor and one of said first and second power supplies, having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a control signal to be controlled to be on and off complementarily with the transistor constituting said first switch circuit.

25. A differential amplifier circuit comprising:

a differential stage including:

a differential pair for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair connected between an output pair of the differential pair and a first power supply, said load element pair comprised of a transistor pair, conductivity type of which is opposite that of a transistor pair composing said differential pair; and

a current source connected between said differential pair and a second power supply and supplying a current to said differential pair; and

an output amplification stage receiving an output of said differential stage and having an output terminal for outputting an output signal, said output amplification stage including an output stage transistor connected between said output terminal and said first power supply;

said differential pair and/or said load element pair being

comprised of transistors each having relatively low threshold value;

a first switch circuit for controlling an activation and deactivation of said differential stage, wherein said switch circuit comprises a transistor connected in series with said current source between said differential pair and a second power supply, having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a control signal to be controlled to be on and off, or said first switch circuit is constituted by said current source comprised of a transistor having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a control signal to be controlled to be on and off;

a transistor connected in series with said output stage transistor between said output terminal and said first power supply, having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving said control signal to be controlled to be on and off in phase with said transistor constituting said first switch circuit.

26. The differential amplifier circuit according to claim 24, further comprising a transistor connected between said output terminal and said second power supply, having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving said control signal to be controlled to be on and off.

27. The differential amplifier circuit according to claim 24, wherein

the conductivity type of said output stage transistor is opposite that of said differential pair.

28. The differential amplifier circuit according to claim 24, wherein said output amplification stage comprises a current source and a transistor having a threshold value higher than that of the transistor having relatively low threshold value connected in series between said output terminal and said second power supply.

29. A differential amplifier circuit comprising:

first and second input terminals;

an output terminal;

a first differential stage including:

a first differential pair for differentially receiving signal voltage supplied to said first and second input terminals;

a first load element pair connected between an output pair of the first differential pair and a first power supply, said first load element pair being comprised of a transistor pair, conductivity type of which is opposite that of a transistor pair composing said first differential pair; and

a first current source connected between said first differential pair and a second power supply and supplying a current to said first differential pair;

a second differential stage including:

a second differential pair for differentially receiving signal voltage supplied to said first and second input terminals, conductivity type of which is opposite that of a transistor pair composing said first

differential pair;

a second load element pair connected between an output pair of the second differential pair and said second power supply, said second load element pair being comprised of a transistor pair, conductivity type of which is opposite that of a transistor pair composing said second differential pair; and

a second current source connected between said second differential pair and said first power supply and supplying a current to said second differential pair;

a first output amplification stage receiving an output of said first differential pair and outputting an output signal from said output terminal;

a second output amplification stage receiving an output of said second differential pair and outputting an output signal from said output terminal;

said first differential pair and/or said first load element pair being comprised of transistors each having relatively low threshold value;

said second differential pair and/or said second load element pair being comprised of transistors each having relatively low threshold value;

a first switch circuit for controlling an activation and deactivation of said differential stage, wherein said first switch circuit includes a transistor connected in series with said first current source between said firs differential pair and said second power supply, having

a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a first control signal for being controlled to be on and off, or said first switch circuit is constituted by said first current source comprised of a transistor having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a bias voltage as said first control signal to be controlled to be on and off; and

a second switch circuit for controlling an activation and deactivation of said differential stage; wherein said second switch circuit includes a transistor connected in series with said second current source between said second differential pair and said first power supply, having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a second control signal for being controlled to be on and off, or said second switch circuit is constituted by said second current source comprised of a transistor having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a bias voltage as said second control signal to be controlled to be on and off.

30. The differential amplifier circuit according to claim 29, wherein

said first output amplification stage includes a first output stage transistor having relatively low threshold value connected between said output terminal and said first power supply;

said second output amplification stage includes a second

output stage transistor having a relatively low threshold value, connected between said output terminal and said second power supply;

a third switch circuit for controlling activation and deactivation of said first output amplification stage, including a transistor connected in series with said first output stage transistor between said output terminal and said first power supply, having a control terminal for a receiving said first control signal for being controlled to be on and off in phase with on and off of said first switch circuit, and having a threshold value higher than that of the transistor having a relatively low threshold value;

a fourth switch circuit for controlling activation and deactivation of said second output amplification stage, including a transistor connected in series with said second output stage-transistor between said output terminal and said second power supply, having a control terminal for a receiving said second control signal for being controlled to be on and off in phase with on and off of said second switch circuit, and having a threshold value higher than that of the transistor having a relatively low threshold value.

31. The differential amplifier circuit according to claim 29, wherein

said first output amplification stage includes a transistor connected between said output terminal and said first power supply, having a threshold value higher than that of the transistor having relatively low threshold value and having a control terminal for receiving a first control signal for being controlled to be on and off in phase with said first switch circuit; and wherein

said second output amplification stage includes a transistor connected between said output terminal and said second power supply, having a threshold value higher than that of the transistor having relatively low threshold value and having a control terminal for receiving a second control signal for being controlled to be on and off in phase with said second switch circuit.

32. The differential amplifier circuit according to claim 29, wherein

said first output stage transistor is a transistor, conductivity of which is opposite that of said first differential pair; and

said second output stage transistor is a transistor, conductivity of which is opposite that of said second differential pair.

33. The differential amplifier circuit according to claim 29, further comprising a circuit for controlling to charge and/or discharge said output terminal at a predetermined timing before the output signal is output from said output terminal.

34. The differential amplifier circuit according to claim 29, wherein

said first output amplification stage includes a current source and a transistor having a threshold value higher than that of the transistor having relatively low threshold value and having a control terminal for receiving said first control signal for being controlled to be on and off in phase with said first switch circuit, connected in series between said output terminal and said second power supply; and wherein

said second output amplification stage includes a current source and a transistor having a threshold value higher than that of the transistor having relatively low threshold value and having a control

terminal for receiving said first control signal for being controlled to be on and off in phase with said second switch circuit, connected in series between said output terminal and said first power supply.

35. A differential amplifier circuit comprising:

a differential pair for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair connected between an output pair of the differential pair and a power supply; and

a current source for supplying a current to said differential pair;

said differential pair, and/or, said load element pair being comprised of transistors each having relatively low threshold value;

wherein said current source is comprised of a transistor having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a bias voltage as a control signal to be controlled to be on and off.

36. A differential amplifier circuit comprising:

a differential pair for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair connected between an output pair of the differential pair and a power supply; and

a current source for supplying a current to said differential pair;

said differential pair and/or said load element pair being comprised of transistors each having relatively low threshold value;

said differential amplifier circuit further comprising a switch circuit for controlling activation and deactivation, wherein switch circuit includes at least one transistor having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a control signal to be controlled to be on and off.

37. The differential amplifier circuit according to claim 36, wherein said load element pair comprises a pair of transistors having control terminals coupled; wherein

said switch circuit comprises a first switch comprised of a transistor having a threshold value higher than that of the transistor having relatively low threshold value, connected between said power supply and said coupled control terminals of said load element pair, and a second switch comprised of a transistor having a threshold value higher than that of the transistor having relatively low threshold value, connected between an output end of one transistor of said load element pair and said coupled control terminals; and wherein

said first and second switches are controlled in common to be on and off by a control signal supplied to control terminals of said transistors constituting said first and second switches.

38. A amplifier circuit comprising:

a follower type transistor having relatively low threshold value, receiving an input signal at a control terminal thereof and outputting from an output terminal thereof an output signal voltage following the control terminal voltage; and

a transistor having a threshold value higher than that of the transistor having relatively low threshold value, connected in series with said follower type transistor between said output terminal and a power supply.

39. The amplifier circuit according to claim 38, comprising a transistor having a threshold value higher than that of the transistor having relatively low threshold value, connected in series with a current source between said output terminal and a second power supply.

40. The differential amplifier circuit according to claim 21, wherein in case of a threshold value of the transistor being negative, high and low of said threshold value corresponds to large and small of an absolute value of a threshold value.

41. The amplifier circuit according to claim 38, wherein in case of a threshold value of the transistor being negative, high and low of said threshold value corresponds to large and small of an absolute value of a threshold value.

42. The differential amplifier circuit according to claim 21, wherein said transistor is composed by a thin film transistor including a crystalline silicon film as an active layer formed on a insulating substrate.

43. The differential amplifier circuit according to claim 21, wherein said transistor is composed by a thin film transistor including a polycrystalline silicon film as an active layer formed on a insulating substrate.

44. The amplifier circuit according to claim 38, wherein said

transistor is composed by a thin film transistor including a crystalline silicon film as an active layer on a insulating substrate.

45. The amplifier circuit according to claim 38, wherein said transistor is composed by a thin film transistor including a polycrystalline silicon film as an active layer formed on a insulating substrate.

46. A memory device comprising a sense amplifier including the differential amplifier circuit as set forth in claim 21.

47. A display device comprising:

a display panel including a plurality of data lines and

a data driver receiving a data signal and driving a data line provided in said display panel, said data driver including the differential amplifier circuit as set forth in claim 21.

48. A semiconductor device including the differential amplifier circuit as set forth in claim 21, said transistor the differential amplifier circuit being composed by a thin film transistor including a crystalline silicon film as an active layer on a insulating substrate.

49. A semiconductor device including the amplifier circuit as set forth in claim 38, said transistor in the amplifier circuit being composed by a thin film transistor including a crystalline silicon film as an active layer on a insulating substrate.

50. The semiconductor device according to claim 48, comprising a plurality of transistors, conductivity type of which are the same, including plural classes of transistors, threshold values of different classes being different; and

a plurality of transistors, conductivity type of which are distinct, including transistors, into channel regions of which same dopant are introduced with approximately an equal dose.

51. The semiconductor device according to claim 48, wherein the transistors with different threshold values include a transistor having a channel region into which dopant of p-type or n-type is introduced; and a transistor having a channel region into which no dopant is introduced.

52. The semiconductor device according to claim 48, wherein the transistors with different threshold values include a transistor having a channel region into which dopant of p-type or n-type is introduced; and a transistor having a channel region into which dopant of p-type and n-type are introduced.

53. The differential amplifier circuit according to claim 24, wherein said transistor is composed by a thin film transistor including a crystalline silicon film as an active layer on a insulating substrate.

54. The differential amplifier circuit according to claim 24, wherein said transistor is composed by a thin film transistor including a polycrystalline silicon film as an active layer formed on a insulating substrate.

55. The differential amplifier circuit according to claim 25, wherein said transistor is composed by a thin film transistor including a crystalline silicon film as an active layer on a insulating substrate.

56. The differential amplifier circuit according to claim 25, wherein said transistor is composed by a thin film transistor including a polycrystalline silicon film as an active layer formed on a insulating

substrate.

57. The differential amplifier circuit according to claim 29, wherein said transistor is composed by a thin film transistor including a crystalline silicon film as an active layer on a insulating substrate.

58. The differential amplifier circuit according to claim 29, wherein said transistor is composed by a thin film transistor including a polycrystalline silicon film as an active layer formed on a insulating substrate.

59. The differential amplifier circuit according to claim 35, wherein said transistor is composed by a thin film transistor including a crystalline silicon film as an active layer on a insulating substrate.

60. The differential amplifier circuit according to claim 35, wherein said transistor is composed by a thin film transistor including a polycrystalline silicon film as an active layer formed on a insulating substrate.

61. The differential amplifier circuit according to claim 36, wherein said transistor is composed by a thin film transistor including a crystalline silicon film as an active layer on a insulating substrate.

62. The differential amplifier circuit according to claim 36, wherein said transistor is composed by a thin film transistor including a polycrystalline silicon film as an active layer formed on a insulating substrate.